Page 9 of 14

#### REMARKS

Applicant appreciates the thorough examination of the present application that is evidenced in the Official Action of January 22, 2004. In response, Applicant has amended each of the independent Claims 1, 10 and 19 to more clearly specify the sequential order of the steps that are recited in the claims, by adding "then" between each step. This sequence was already inherent in the claims, so that these amendments are not narrowing amendments, and the full range of equivalents is available for these claims. As will be described in detail below, even assuming for the sake of argument that the layer 25 of Biolsi et al. and the layer 501 of Stamper are interpreted as suggested by the Official Action, neither of these references nor their combination would describe or suggest the sequence of steps recited in the independent claims. Moreover, many of the dependent claims are separately patentable.

### **Affirmation of Election**

Applicant hereby affirms the oral election of Invention I, corresponding to Claims 1-17 and 19-23. The Invention II claims (Claims 18 and 24-28) have been withdrawn without prejudice to the filing of a divisional application. This affirmation is being made without traverse because Applicant agrees that patentably distinct inventions are present. The title has been changed to conform to the elected method claims. To the extent necessary, this Affirmation shall also constitute an Interview Summary pursuant to MPEP 713.04

## Claims 1, 4-6 and 8-9 Are Patentable Over Biolsi et al.

Claims 1, 4-6 and 8-9 stand rejected under 35 USC §102(e) as being anticipated by U.S. Patent Application Publication No. US 2002/0177301 A1 to Biolsi et al. Applicant respectfully submits that these claims are patentable for at least the reasons that will now be described.

In particular, independent Claim 1 recites:

1. A method for forming a dual damascene metal interconnection of a semiconductor device, comprising:

forming an interlayer insulation layer and a polishing buffer layer on a semiconductor substrate; then

Page 10 of 14

etching the interlayer insulation layer and the polishing buffer layer to form a via hole; then

forming a sacrificial filling film on the polishing buffer layer to fill the via hole; then

etching the sacrificial filling film, the polishing buffer layer and the interlayer insulation layer to form a trench, thereby forming a dual damascene pattern including the via hole and the trench; then

forming an etching buffer layer on a sidewall of the trench; then removing at least some of the sacrificial filling film in the via hole; and then

forming a metal interconnection within the dual damascene pattern. In Paragraph 8, the Detailed Action states that Biolsi et al.'s layer 25 may serve as the claimed etching buffer layer in the broadest interpretation.

However, even assuming the broadest interpretation of "an etching buffer layer" in Claim 1, Claim 1 recites that the step of "forming an etching buffer layer on a sidewall of the trench" takes place after the step of "etching the sacrificial filling film, the polishing buffer layer and the interlayer insulation layer to form a trench", and before the step of "removing at least some of the sacrificial filling film in the via hole". In contrast, Biolsi et al.'s thin liner layer 25 is formed after the sacrificial filling film is removed in the via hole. More specifically, the thin liner layer 25 is formed in Biolsi et al. Figure 12a after the sacrificial filling film is removed in the via hole 24 in Figures 10 and 11. See, for example, Biolsi et al. Paragraphs [0064] to [0068]. Accordingly, even using the broadest interpretation of Applicant's step of "forming an etching buffer layer on the sidewall of the trench", Biolsi et al. does not describe the claimed sequence of steps in Claim 1. For at least these reasons, Claim 1 is not anticipated by Biolsi et al.

Dependent Claims 4-6 and 8-9 also are patentable by virtue of the patentability of independent Claim 1 from which they depend. Moreover, many of these claims are independently patentable. In particular, Claim 8 recites that the last step of Claim 1 "forming a metal interconnection within the dual damascene pattern" comprises:

depositing a barrier metal film and a metal film to fill the dual damascene pattern including the etching buffer layer; and

etching the barrier metal film and the metal film through a chemical mechanical polishing process using the polishing buffer layer to form the metal interconnection including a dual barrier metal film.

Applicant respectfully submits that if the thin liner 25 of Biolsi et al. is construed as being an etching buffer layer, then Biolsi et al. does not describe any separate step of

Page 11 of 14

depositing a barrier metal film and etching the barrier metal film, as recited in Claim 8. Stated differently, the formation of the thin liner 25 in Figure 12a of Biolsi et al. cannot satisfy both the step of forming an etching buffer and the step of depositing a barrier metal film. Accordingly, Claim 8, and Claim 9 that depends therefrom, are independently patentable.

### Claims 1-17 and 19-23 Are Unobvious

Claims 1-17 and 19-23 stand rejected under 35 USC §103 over Biolsi et al. in view of U.S. Patent 6,297,149 to Stamper. In this regard, Applicant wishes to point out that, to establish a prima facie case of obviousness, three basic criteria must be met. The prior art reference (or references when combined) must teach or suggest all the claim limitations. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, and there must be a reasonable expectation of success of the combination. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. See MPEP § 2143. As affirmed by the Court of Appeals for the Federal Circuit, to support combining references in a §103 rejection, evidence of a suggestion, teaching, or motivation to combine must be clear and particular, and this requirement is not met by merely offering broad, conclusory statements about teachings of references. *In re* Dembiczak, 50 USPQ2.d 1614, 1617 (Fed. Cir. 1999). The Court of Appeals for the Federal Circuit has also stated that, to support combining or modifying references, there must be particular evidence from the prior art as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. In re Kotzab, 55, USPQ2d 1313, 1317 (Fed. Cir. 2000).

In particular, as was already described in connection with Claim 1 above, even assuming that Biolsi et al.'s thin liner 25 is an etching buffer, Biolsi et al.'s thin liner 25 is formed after removing the sacrificial filling film in the via hole, rather than before removing the sacrificial filling film in the via hole, as recited in Claim 1. This missing teaching is simply not described or suggested by Stamper. In particular, in

Page 12 of 14

Stamper, the Official Action states that the etching buffer layer corresponds to layer 501 of, for example, Stamper's Figures 5A-5F. However, as shown in Stamper Figure 5A, layer 501 is formed prior to forming a sacrificial filling film and prior to forming a trench. Yet Claim 1 recites that the etching buffer layer is formed after both of these steps. Moreover, as clearly shown in Figures 5D-5F, the layer 501 simply is not present on the sidewall of the trench 507. Yet Claim 1 recites "forming an etching buffer layer on a sidewall of the trench".

Accordingly, even if the references were combined, the combination would not describe or suggest "forming an etching buffer layer on a sidewall of the trench" in the sequence recited in Claim 1. Biolsi et al. might suggest this step after removing the sacrificial filling film in the via hole, whereas Stamper might suggest this step prior to forming a sacrificial filling film on the polishing buffer layer to fill the via hole. Their combination would suggest forming an etching buffer after removing at least some of the sacrificial filling film in the via hole, but before forming a sacrificial filling film on the polishing buffer layer to fill the via hole. Therefore, the combination would not describe or suggest:

forming a sacrificial filling film on the polishing buffer layer to fill the via hole; then

etching the sacrificial filling film, the polishing buffer layer and the interlayer insulation layer to form a trench, thereby forming a dual damascene pattern including the via hole and the trench; then

forming an etching buffer layer on a sidewall of the trench; then removing at least some of the sacrificial filling film in the via hole; and then

forming a metal interconnection within the dual damascene pattern, as recited in Claim 1.

Independent Claim 10 includes similar recitations:

etching the sacrificial filling film, the polishing buffer layer, the second interlayer insulation layer and the second etch stop layer to form a trench, thereby forming a dual damascene pattern including the via hole and the trench; then

forming an etching buffer layer on a sidewall of the trench; then removing a remaining sacrificial filling film in the via hole; then removing the first etch stop layer within the via hole; and then forming a metal interconnection within the dual damascene pattern.

By similar reasoning, the combination of Biolsi et al. and Stamper does not describe or suggest these recitations.

Page 13 of 14

# Finally, Claim 19 recites:

19. A method of forming a metal interconnection for an integrated circuit device, comprising:

forming a trench in an integrated circuit substrate and a via hole beneath a portion of the trench, the trench including a trench sidewall and the via hole including a sacrificial film therein; then

forming a buffer layer on the trench sidewall; then

removing at least some of the sacrificial film from the via hole by etching the sacrificial film through the trench that includes the buffer layer on the trench sidewall; and then

forming the metal interconnection in the via hole from which at least some of the sacrificial film has been removed, and in the trench.

Again, with respect to Claim 19, taking the buffer layer in its broadest interpretation offered by the Examiner, Biolsi et al. might suggest forming the buffer layer on a trench sidewall after removing the sacrificial film and Stamper might suggest forming the buffer layer prior to forming the trench and, in any event, would not suggest forming the buffer layer on the trench sidewall at all.

Accordingly, independent Claims 1, 10 and 19 are patentable over Biolsi et al. in view of Stamper. Dependent Claims 2-9, 11-17 and 20-23 are patentable at least per the patentability of the base claim from which they depend.

Moreover, many of the dependent claims are separately patentable. In particular, Claims 3, 4, 5, 6, 11, 12, 13, 14, 20 and 21 recite properties of the etching buffer layer that cause it to act as an etching buffer layer. Since these claims recite that the etching buffer layer is a protective layer, they are separately patentable. In particular, Applicant respectfully submits that Biolsi et al.'s thin liner 25 would not act as a protective layer for the sidewall of the trench, because it is formed after the via and trench are etched at Figures 10 and 11 of Biolsi et al. Moreover, Stamper's layer 501 would not act as a protective layer for the sidewall of the trench, because it is simply not on the sidewall of the trench. As noted in the present application, for example at Page 4, lines 12-13, by providing the buffer layer as a protective layer on the sidewall of the trench, necking or other flaws may be reduced or prevented. For at least these reasons, these dependent claims are separately patentable.

Page 14 of 14

# Petition to Accord Proper Filing Date

Applicant filed a "Petition to Accord the Proper Filing Date" on December 22, 2003. The U.S. Patent and Trademark Office electronic file wrapper for the present application indicates that this Petition is part of the electronic file wrapper. However, this Petition has not yet been acted upon. Accordingly, Applicants respectfully request action on this Petition, and according of the proper filing date of August 20, 2003 for the present application.

### **Conclusion**

Applicant again wishes to thank the Examiner for the thorough examination of the application. However, Applicant has now shown that even if the layers of the independent claims are interpreted as broadly as possible, the prior art simply does not suggest the sequence of steps that is recited in the independent claims. Moreover, the dependent claims recite functionality that is neither described nor suggested by the prior art. Accordingly, Applicant respectfully requests withdrawal of the outstanding rejections and allowance of the present application.

Respectfully submitted.

Mitchell S. Bigel Registration No. 29,614 Attorney for Applicants

**Customer Number 20792** 

Myers Bigel Sibley & Sajovec, P.A. P.O. Box 37428 Raleigh, NC 27627 919-854-1400 919-854-1401 (Fax)

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 21, 2004,

Susan E. Freedman

Date of Signature: April 21, 2004